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10/580,346	03/16/2007	Akihiko Namba	050212-0716	3240

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
4146	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,346	NAMBA ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *9,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/25/2006, 03/16/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9, 15, and 16 are objected to because of the following informalities:

a. Regarding claim 9, “the donor element" lacks antecedent basis.

b. Regarding claims 15 and 16, the claims invoke a method claim that is dependent on a device claim, which renders the scope of the claim as indefinite.

Appropriate correction is required.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: a second semiconductor layer, which is necessary for device operation.

5. A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 1 recites the broad recitation of a “temperature region from 0°C to 300°C”, and the claim also recites “a temperature range of at least 100°C”, which is the narrower statement of the range/limitation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 6, 8, and 13 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ando et al. (JP 2001-007385).

a. Regarding claim 1 – 6 and 8, Ando discloses a diamond n-type semiconductor (e.g. figure 3c) comprising a first diamond semiconductor having n-type conduction (semiconductor layer 7, disclosed in paragraph [0018]) wherein, in said first diamond semiconductor, a conductor exhibits an electron concentration negatively correlated with temperature in a temperature range of at least 100°C within at least the temperature region from 0°C to 300°C

wherein, in said first diamond semiconductor, the conductor exhibits a Hall coefficient positively correlated with temperature in a temperature range of at least 100°C within at least the temperature region from 0°C to 300°C

wherein the temperature range exists over at least 200°C within at least the temperature region from 0°C to 300°C

wherein said first diamond semiconductor has a resistivity of 500 Ωcm or less at least at a temperature within the temperature region from 0°C to 300°C

wherein the electron concentration of said first diamond semiconductor is always at least 10^{16} cm^{-3} in the temperature region from 0°C to 300°C

wherein said first diamond semiconductor contains more than 5 x 10^{19} cm^{-3} in total of at least one kind of donor element (paragraph [0018] discloses a dopant concentration to be between 1 x 10^{13} cm^{-3} and 1 x 10^{21} cm^{-3})

wherein said first diamond semiconductor contains at least S (sulfur) as the donor element (paragraph [0018] discloses the dopant of layer 7 to be sulfur).

(device of figure 3c contains an n-type diamond semiconductor layer containing a concentration sulfur dopant, as disclosed in paragraph [0018], which resides on a pure (insulating) layer of diamond (layer 3) as disclosed in paragraphs [0020] and [0032]. Since the device of Ando meets the structural limitations of the invention as disclosed by the applicant in the specification and claims, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claims 1 - 5, are inherent to the device of Ando).

b. Regarding claim 13, Ando discloses a semiconductor device at least partly employing a diamond n- type semiconductor according to claim 1 (figure 3c, using the invention of claim 1, as cited above, is a semiconductor device used to emit ultraviolet rays, as disclosed in the abstract and paragraph [0014]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Hasegawa et al. (US 2002/0127405). Ando discloses a diamond n-type semiconductor according to claim 6, as cited above, however Ando is silent with respect to said first diamond semiconductor containing at least P (phosphorus) as the donor element. Hasegawa discloses that diamond n-type semiconductors may be produced with Phosphorus as the donor element in a concentration range of $1x\ 10^{16}$ to $1x10^{21}$ cm^{-3} (paragraph [0037] - [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the diamond layer of Ando such that the donor element is phosphorus because it was well-known in the art that phosphorus can be used as a dopant in n-type diamond semiconductor layers, as disclosed by Hasegawa. One would be motivated to use phosphorus as the donor element because it produces an n-type semiconductor when doped with diamond, with properties that are well known and studied within the art.

10. Claims 9, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Yoshida (US 6,340,393).

a. Regarding claim 9, Ando discloses a diamond n-type semiconductor according to claim 1, as cited above, however Ando is silent with respect to said first diamond semiconductor containing an impurity element other than the donor element together with the donor element. Yoshida discloses a combining a second impurity element together with the donor element in a diamond semiconductor (col. 2, lines 51 – 52, col. 5, lines 59 – 61, and col. 5, lines 65 - 67).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the invention of Ando to include a second impurity element along with the donor element, as principally taught by Yoshida, because such a layer because it would allow for an increase in donor density for a given temperature range (as disclosed in table 1 of Yoshida).

b. Regarding claim 11, Ando discloses a diamond n-type semiconductor according to claim 1, as cited above, but is silent with respect to the said first diamond semiconductor being a monocrystal diamond. Yoshida discloses that a single crystal diamond can be used for a diamond semiconductor (col. 5, lines 59 – 60).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the invention of Ando such that the diamond semiconductor layer is a monocrystal, as taught by Yoshida. One would be motivated to make such a layer because it would imply less crystal defects and

create a cleaner electrical signal and more predictable results stemming from the dopant characteristics.

c. Regarding claim 14, Ando discloses the diamond n-type semiconductor according to claim 1, as cited above, but is silent with respect to the device being used in at least an electron emitting part of an electron emitting device. Yoshida discloses that diamond semiconductor devices can be used as an electron emitter (col. 5, lines 18 – 19).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use the diamond semiconductor of Ando as an electron emitter since Yoshida discloses that such semiconductor devices can be used as electron emitters. One would be motivated to use the devices in such a manner since a low resistivity exists in such devices, creating an efficient electron emitter.

d. Regarding claim 15, Ando discloses a method of manufacturing a diamond n-type semiconductor according to claim 1, as cited above, said method comprising the steps of preparing a diamond substrate (e.g. figure 3c, diamond substrate 3) and epitaxially growing said first diamond semiconductor on said diamond substrate (e.g. figure 3c, semiconductor layer 7, epitaxially formed, as discloses in paragraph [0032]). Ando is silent with regards to introducing an impurity element other than a donor element to said diamond substrate. Yoshida

discloses introducing an impurity element other than a donor element to the diamond substrate (e.g. figure 3 and col. 2, lines 49 – 51).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Ando to include a method of introducing a second impurity element along with the donor element because Yoshida discloses a method of forming diamond semiconductor with such a structure. One would be motivated to use such a method to make a layer because it would allow for an increase in donor density for a given temperature range (as disclosed in table 1 of Yoshida).

11. Claims 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando and Yoshida as applied to claims 9 and 15 above, respectively, and further in view of Hasegawa.

a. Regarding claim 10, Ando, in view of Yoshida, disclose a diamond n-type semiconductor according to claim 9, as cited above, however they are silent with respect to said first diamond semiconductor containing at least 1 x 10^{17} cm^{-3} of Si as the impurity element. Hasegawa discloses that a concentration of 1x 10^{16} to 1x10^{21} cm^{-3} of silicon can be used as an impurity element when doping semiconductor diamond (paragraphs [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Ando, in view of Yoshida, such that the other impurity element is silicon with a concentration of 1x 10^{16} to 1x10^{21}

cm^{-3} since Hasegawa discloses that silicon can be used in such concentrations to dope semiconductor diamond. One would be motivated to use silicon as an impurity element since silicon was a commonly used element in the semiconductor industry and is readily available with well-known properties.

b. Regarding claim 16, Ando, in view of Yoshida, discloses a method of manufacturing a diamond n-type semiconductor according to claim 15, as cited above, however they are silent with respect to Si being artificially introduced as the impurity element to said diamond substrate. Hasegawa discloses that silicon can be used as an impurity element when doping semiconductor diamond (paragraphs [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Ando, in view of Yoshida, such that the impurity element is silicon since Hasegawa discloses that silicon can be used to dope diamond. One would be motivated to use silicon as an impurity element since silicon was a commonly used element in the semiconductor industry and is readily available with well-known properties.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Komuro (US 6,204,543 B1). Ando discloses a diamond n-type semiconductor according to claim 1, as cited above, further comprising a second diamond semiconductor provided adjacent to said first diamond semiconductor (e.g. figure 3c,

diamond semiconductor layer 5, as disclosed in paragraph [0017]). Ando is silent with respect to the second diamond semiconductor being n-type and in said second diamond semiconductor, a conductor exhibits an electron concentration not negatively correlated with temperature and a Hall coefficient not positively correlated with temperature. Komuro discloses the use of n-type semiconductors adjacent to each other in which there is a highly doped region and a less-doped region (e.g. figure 2F, low density regions 8 and 6 and high density region 11, as disclosed in col. 3 lines 57 – 63, col. 4 lines 1 - 9, and col. 4 lines 18 - 27. The structural limitations of the layers are such that the lower density region exhibits an electron concentration not negatively correlated with temperature and a Hall coefficient not positively correlated with temperature.)

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Ando such that the second diamond semiconductor layer is an n-type layer with a low density of dopants since it was taught by Komura to make multiple n-type semiconductor layers. One would be motivated to make such a device since the electric field between separately doped n-type semiconductor is less abrupt than between adjacent p-type and n-type semiconductors, resulting in a more moderate electron energy and more reliable device, as discussed in the Description of the Related Art of Komuro.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is

(571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 4146
February 12, 2008

/Marvin M. Lateef/
Supervisory Patent Examiner, Art Unit 4146